

CLAIMS

I claim:

- 5 1. A method of forming a bond pad, the method comprising:
 - a) depositing a dielectric layer on a substrate;
 - b) depositing a photoresist layer on the dielectric layer;
 - c) forming an etch mask in the photoresist layer wherein the mask includes
10 (1) a first mask section for etching a bond pad hole and (2) a second mask
 section for etching a trench, wherein the first and second mask sections
 are contiguous;
 - d) etching the first and second mask sections through the dielectric layer,
 wherein a bond pad hole and a contiguous trench are formed, such that the
 bond pad hole and the trench expose a section of the substrate; and
15 e) forming a layer comprising Cu, in the pad hole and in the trench, wherein
 a bond pad having a contiguous interconnect line is formed.
- 20 2. The method of claim 1 additionally comprising:
 - a) depositing a passivation layer on (1) the dielectric layer, (2) the bond pad
 and (3) the contiguous interconnect line; and
 - b) forming a passivation hole through the passivation layer such that the
 passivation hole exposes at least a portion of the bond pad.
- 25 3. The method of claim 1 wherein the substrate comprises a top layer including
 a C-doped silicon oxide material.
- 30 4. The method of claim 3 wherein the C-doped silicon oxide material comprises
 an oxidized organo silane material including an oxidized organo silane
 compound that is formed by reacting an organo silane compound with an
 oxidizing compound.
5. The method of claim 4 wherein the oxidized organo silane material comprises
 a carbon content of at least 1% by atomic weight.

6. The method of claim 5 wherein the oxidized organo silane material is formed by reacting an organo silane compound with N_2O gas at plasma conditions sufficient to form top the layer and wherein the plasma conditions additionally comprise:
- 5 a) a high frequency RF power density ranging from about 0.16 W/cm^2 to about 0.48 W/cm^2 for forming the layer; and
- b) a sufficient amount of organo silane compound with respect to the N_2O gas to form the layer.
- 10 7. The method of claim 5 wherein the oxidized organo silane material is formed by reacting an organo silane compound with O_2 gas at plasma conditions sufficient to form the layer and wherein the plasma conditions comprise:
- a) a high frequency RF power density greater than about 0.03 W/cm^2 for forming the layer; and
- 15 b) a sufficient amount of organo silane compound with respect to the O_2 gas to form the layer.
8. The method of claim 1 wherein the substrate comprises an IC structure.
- 20 9. The bond pad formed according to the method of claim 2.
10. A method of forming a wire bond pad, the method comprising:
- a) depositing a first dielectric layer on an IC structure;
- b) depositing a second dielectric layer on the first dielectric layer;
- 25 c) depositing a photoresist layer on the second dielectric layer;
- d) forming an etch mask in the photoresist layer wherein the mask includes (1) a first mask section for etching a bond pad hole and (2) a second mask section for etching a trench, wherein the first and second mask sections are contiguous;
- 30 e) etching the first and second mask sections through the second dielectric layer, wherein a bond pad hole and a contiguous trench are formed, such the bond pad hole and trench expose a section of the first dielectric layer;
- f) forming a layer comprising Cu, in the pad hole and in the trench, wherein a bond pad having a contiguous interconnect line is formed;

- g) depositing a passivation layer on (1) the second dielectric layer, (2) the bond pad and (3) the contiguous interconnect line;
- h) forming a passivation hole through the passivation layer such that the passivation hole exposes at least a portion of the bond pad;
- 5 i) depositing a plug comprising Al in the passivation hole; and
- j) fabricating a bond pad comprising Al on the plug and on a portion of the passivation layer, thereby forming the wire bond pad.

11. The wire bond pad formed according to the method of claim 10.

12. A method of forming a duplex bond pad, the method comprising:

- a) depositing a dielectric layer on an IC substrate;
- b) forming a bond pad hole in the dielectric layer;
- c) fabricating a Cu bond pad in the bond pad hole;
- 15 d) depositing a passivation layer on the dielectric layer including the bond pad;
- e) forming at least two via holes in the passivation layer such that the at least two via holes expose at least a section of the Cu bond pad;
- f) depositing an Al material into the two or more via holes, thereby forming two or more via plugs; and
- 20 g) fabricating an Al wire bond pad on the passivation layer and on the two or more via plugs, thereby forming a duplex bond pad wherein the Cu bond pad and the Al wire bond pad are connected through the two or more via plugs.

13. The duplex bond pad formed according to the method of claim 12.

14. A method of forming a duplex bond pad, the method comprising:

- a) depositing a dielectric layer on an IC structure;
- 30 b) depositing a photoresist layer on the dielectric layer;
- c) forming an etch mask in the photoresist layer wherein the mask includes (1) a first mask section for etching a bond pad hole and (2) a second mask section for etching a trench, wherein the first and second mask sections are contiguous;

- d) etching the first and second mask sections through the dielectric layer, wherein a bond pad hole and a contiguous trench are formed, such that the bond pad hole and trench expose a section of the IC structure;
- e) forming a layer comprising Cu, in the pad hole and in the trench, wherein a bond pad having a contiguous interconnect line is formed;
- f) depositing a passivation layer on (1) the dielectric layer, (2) the bond pad and (3) the contiguous interconnect line;
- g) forming at least two via holes through the passivation layer such that the via holes expose at least first and second sections of the bond pad;
- h) forming via plugs comprising Al in the at least two via holes; and
- i) fabricating a bond pad comprising Al on the via plugs and on a portion of the passivation layer, thereby forming the duplex bond pad.

15. The duplex bond pad formed according to the method of claim 14.

16. A method of forming a bond pad, the method comprising:

- a) depositing a first dielectric layer on a first IC structure;
- b) depositing a second dielectric layer on the first dielectric layer;
- c) depositing a photoresist layer on the second dielectric layer;
- d) forming an etch mask in the photoresist layer wherein the mask includes (1) a first mask section for etching a bond pad hole and (2) a second mask section for etching a trench, wherein the first and second mask sections are contiguous;
- e) etching the first and second mask sections through the second dielectric layer, wherein the bond pad hole and the contiguous trench are formed, such that the bond pad hole and the trench expose a section of the first dielectric layer;
- f) forming an electrically conductive liner in the bond pad hole and in the contiguous trench, thereby forming a lined pad hole and a lined contiguous trench;
- g) forming a layer comprising Cu, in the lined pad hole and in the lined contiguous trench, such that the layer comprising Cu provides an underfill of the pad hole and the trench;

- h) forming a metal overcoat layer on the Cu layer such that the metal overcoat layer provides an overfill of the pad hole and the trench, wherein a second IC structure is formed; and
- i) planarizing the second IC structure to define a bond pad having (1) a bond pad top surface (2) an overcoat layer comprising at least 95% of the bond pad top surface and (3) a contiguous interconnect line having (i) a line top surface and (ii) an overcoat layer comprising at least 95% of the line top surface.

5

10

17. The method of claim 16 additionally comprising:

- a) depositing a passivation layer on (1) the second dielectric layer, (2) the bond pad and (3) the contiguous interconnect line; and
- b) forming a passivation hole through the passivation layer such that the passivation hole exposes at least a section of the bond pad.

15

18. The method of claim 16 wherein the first dielectric layer comprises a C-doped silicon oxide layer.

20

19. The method of claim 16 wherein forming the electrically conductive liner comprises forming a sandwich layer including:

- a) depositing a substantially conformal Cu diffusion barrier layer in the pad hole and in contiguous trench; and
- b) depositing a substantially conformal Cu seed layer on the Cu diffusion barrier layer.

25

20. The method of claim 16 wherein forming a metal overcoat layer is selected from the methods consisting of electroless metal deposition and electroplate metal deposition.

30

21. The bond pad formed according to the method of claim 16.

22. A method of forming a bond pad, the method comprising:

- a) depositing a first dielectric layer on an IC structure;
- b) depositing a second dielectric layer on the first dielectric layer;

- c) employing etching techniques for etching (1) a pad hole and a contiguous trench through the second dielectric layer and (2) a via hole through the first dielectric layer, wherein the via hole connects the trench with the IC structure; and

- 5 d) employing a dual damascene technique for simultaneously forming (1) a via plug comprising Cu, (2) a bond pad comprising Cu and (3) a contiguous interconnect line comprising Cu.

23. The method of claim 22 additionally comprising:

- 10 a) depositing a passivation layer on (1) the second dielectric layer, (2) the bond pad and (3) the contiguous interconnect line; and
- b) forming a passivation hole through the passivation layer such that the passivation hole exposes at least a section of the bond pad.

15 24. The bond pad formed according to the method of claim 22.

25. A method of forming a bond pad, the method comprising:

- a) depositing a first dielectric layer on a first IC structure;
- b) depositing a second dielectric layer on the first dielectric layer;
- 20 c) employing etching techniques for etching (1) a pad hole and a contiguous trench through the second dielectric layer and (2) a via hole through the first dielectric layer, wherein the via hole connects the trench with the IC structure;
- d) depositing an electrically conductive, substantially conformal Cu diffusion layer inside (1) the via hole, (2) the pad hole and (3) the contiguous trench;
- 25 e) depositing an electrically conductive, substantially conformal Cu seed layer on the Cu diffusion layer, wherein a lined via hole, a lined pad hole and a lined contiguous trench are formed;
- 30 f) employing a dual damascene technique for simultaneously forming a layer comprising Cu (1) inside the lined via hole (2) inside the lined pad hole, and (3) inside the lined contiguous trench, and wherein the layer comprising Cu includes an underfill of the pad hole and the trench;

- g) forming a metal overcoat layer on the layer comprising Cu such that the overcoat layer comprises an overfill of the pad hole and the trench, wherein a second IC structure is formed;
 - h) planarizing the second IC structure to define a bond pad having (1) a bond pad top surface and (2) an overcoat layer comprising at least 95% of the top surface of the bond pad and (3) side and bottom surfaces that are formed in the lined pad hole;
 - i) depositing a passivation layer on (1) the surface of the second dielectric layer, (2) the bond pad and (3) the contiguous interconnect line, and
 - j) forming a passivation hole through the passivation layer such that the passivation hole exposes at least a section of the bond pad.
26. The method of claim 25 wherein forming a metal overcoat layer comprises an electroless deposition method.
27. The method of claim 25 wherein forming the metal overcoat layer comprises an electroplate deposition method.
28. The method of claim 25 wherein the first dielectric layer comprises a C-doped silicon oxide layer.
29. The method of claim 28 wherein the C-doped silicon oxide layer comprises an oxidized organo silane layer including an oxidized organo silane compound that is formed by reacting an organo silane compound with an oxidizing compound.
30. The method of claim 29 wherein the oxidized organo silane layer comprises a carbon content of at least 1% by atomic weight.
31. The bond pad formed according to the method of claim 25.
32. A method of forming a bond pad, the method comprising:
- a) depositing a first dielectric layer on a first IC structure;
 - b) depositing a second dielectric layer on the first dielectric layer;

- c) depositing a photoresist layer on the second dielectric layer;
- d) forming an etch mask in the photoresist layer wherein the mask includes (1) a first mask section for etching a bond pad hole and (2) a second mask section for etching a trench, wherein the first and second mask sections are contiguous;
- e) etching the first and second mask sections through the second dielectric layer, wherein the bond pad hole and the contiguous trench are formed, such that the bond pad hole and the trench expose a section of the first dielectric layer;
- f) forming an electrically conductive barrier/seed liner in the bond pad hole and in the contiguous trench, thereby forming a lined pad hole and a lined contiguous trench;
- g) forming a layer comprising Cu, in the lined pad hole and in the lined contiguous trench, such that the layer comprising Cu provides an overfill of the pad hole and the trench, wherein a second IC structure is formed;
- h) planarizing the second IC structure to define (1) a bond pad portion including a bond pad Cu surface and (2) a contiguous interconnect line portion including a line Cu surface; and
- i) employing an electroless metal deposition technique for depositing a metal overcoat layer on the Cu surface of the bond pad portion and on the Cu surface of the interconnect line portion, wherein a bond pad and contiguous interconnect line are formed.

33. The method of claim 32 additionally comprising:

- a) depositing a passivation layer on (1) the bond pad, (2) the contiguous interconnect line and (3) the second dielectric layer; and
- b) forming a passivation hole in the passivation layer such that the passivation hole exposes at least a section of the metal overcoat layer on the bond pad.

34. A third IC structure formed according to the method of claim 33.

35. A method for forming a solder bump, the method comprising:

- 5 a) forming a bond pad in a dielectric layer, such that the bump pad is exposed;
- b) depositing a passivation layer on the bump pad and the dielectric layer;
- c) forming a plurality of via holes through the passivation layer such that each of the plurality of holes exposes at least a section of the bond pad; and
- d) simultaneously fabricating (1) via plugs in each of the plurality of via holes and (2) a solder bump formed on the via plugs.
- 10 36. The method of claim 35 comprising the bond pad additionally having (1) a top surface and (2) a metal overcoat layer, comprising at least 95% of the top surface, upon which the via holes are formed.
37. A structure comprising:
- 15 a) an IC structure;
- b) a first dielectric layer deposited on the IC structure;
- c) a second dielectric layer deposited on the first dielectric layer;
- d) a bond pad fabricated in the second dielectric layer such that bond pad includes a contiguous interconnect line wherein the bond pad and
- 20 interconnect line contact the first dielectric layer;
- e) a passivation layer covering (1) the second dielectric layer, (2) the interconnect line and (3) the bond pad; and
- f) a passivation hole through the passivation layer, such that the passivation hole exposes at least a portion of the bond pad.
- 25 38. The structure of claim 37 wherein the bond pad additionally comprises:
- a) a bond pad top surface;
- b) bond pad side and bottom surfaces;
- c) a metal overcoat layer comprising at least 95% of the top surface; and
- 30 d) an electrically conductive barrier/seed sandwich layer that substantially covers the bottom and side surfaces.
39. The structure of claim 37 wherein the first dielectric layer comprises a C-doped silicon oxide layer.

40. A duplex bond pad comprising:

- a) an IC structure;
- b) a dielectric layer deposited on the IC structure;
- 5 c) a Cu bond pad formed in the dielectric layer;
- d) a passivation layer deposited on the Cu bond pad and on the dielectric layer;
- e) at least two via plugs formed through the passivation layer, wherein the at least two via plugs contact the Cu bond pad; and
- 10 f) an Al wire bond pad fabricated on (1) the passivation layer and (2) the at least two via plugs.